REMARKS

This is a full and timely response to the outstanding nonfinal Office Action mailed July 31, 2002. Claims 1-10, 17, 18 and 20 remain pending in the present application.

Present Status of Patent Application

Claims 1-10, 17, 18 and 20 have been preliminarily rejected under 35 U.S.C. § 103(a). Applicants traverse all of the rejections of the Office Action. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

I. Response to § 103 Rejections

Claims 1-5, 17, 18 and 20 have been preliminarily rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant Admitted Prior Art (Figs. 1-2) in view of U.S. Patent No. 6,043,704, to Yoshitake (hereafter *Yoshitake*). Claims 6-10 have been preliminarily rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant Admitted Prior Art (Figs. 1-2) in view of *Yoshitake* and further in view of U.S. Patent No. 6,140,686, to Mizuno, *et al.* (hereafter *Mizuno*).

In order for a claim to be properly rejected under 35 U.S.C. § 103, the combined teachings of the prior art references must suggest all features of the claimed invention to one of ordinary skill in the art. *See, e.g., In re Dow Chemical*, 5 USPQ2d1529, 1531 (Fed. Cir. 1988), and *In re Keller*, 208 USPQ2d871, 881 (CCPA 1981). As set forth below, features of the claimed invention are not taught or suggested as indicated in the Office Action and, therefore, Applicants respectfully assert that the claims are in condition for allowance.

Claim 1

Claim 1 recites:

> 1. An integrated circuit comprising:
> a first port for outputting a signal;
> a second port for receiving said signal;
> ***a common area comprising an alignment link for electrically connecting said first port with said second port;***
> ***said first port extends directly into said common area from a first area;***
> ***said second port extends directly into said common area from a second area;*** and

said alignment link comprises a signal buffer for buffering a signal traveling along said alignment link between said first port and said second port.

(Emphasis Added)

Applicants respectfully submit that the combination of Applicant Admitted Prior Art and *Yoshitake* fails to teach, disclose or suggest at least the above-emphasized elements. Particularly, the combination fails to teach, disclose or suggest the elements of a common area comprising an alignment link for electrically connecting a first port with a second port, the first port extending directly into the common area from a first area, and the second port extending directly into the common area from a second area.

In preliminarily rejecting claim 1, the Office Action recites:

Regarding claims 1 and 17, Applicant Admitted Prior Art disclose an integrated circuit (Figs. 1 and 2) comprising:

a first port 10-13 for outputting a signal;

a second port 14, 15, 16 and 17 for receiving the signal;

a common area 35 comprising an alignment link 30, 31, 32 and 33 for electrically connecting the first port with the second port;

the second port extends directly into the common area from a second area;

the alignment link comprises a signal buffer for buffering a signal traveling along the alignment link between the first port and the second port. However, Applicant Admitted Prior Art (Figs. 1 and 2) fail to disclose the first port extends directly into the common area from a first area.

Yoshitake discloses a clock distribution circuit for a semiconductor integrated circuit comprising:

an input driver 11 for outputting a signal; a buffer 12 for receiving an output of the driver 11 (fig. 1, column 7, lines 10-20), wherein the driver 11 extends directly from the first area into the buffer 12 to provide a clock distribution circuit and can realize reduction in skew. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Applicant Admitted Prior Art (Figs. 1 and 2) to provide the driver 11 extends directly from the first area into the buffer 12, as shown by Yoshitake to make a direct contact and avoid the links.

(Office Action, pp. 2-3)

As noted above, the Office Action admits that Applicant Admitted Prior Art (Figs. 1 and 2) fails to disclose the first port extending directly into a common area from a first area. In this regard, the Office Action refers to *Yoshitake*. However, *Yoshitake* does not teach, disclose or suggest the element of a first port extending directly into a common area. Instead, *Yoshitake* discloses a clock distribution circuit for a semiconductor integrated circuit

comprising an input driver 11 for receiving a clock signal from the outside, which the input driver 11 is connected to a first buffer 12 where the connection crosses over a real estate 24. The input driver 11 is connected to the first buffer 12 by clock wiring line 19 so that an output of the input driver 11 is input into the first buffer 12 over the clock wiring line 19 (column 7, lines 22-26).

Yoshitake clearly does not teach, disclose or suggest a first port extending directly into a common area from the first area. Instead, Fig. 1 of *Yoshitake* shows a wiring diagram of a circuit and not a physical layout of the circuit. *Yoshitake* discloses an input driver 11 by clock wiring line 19 extending over a real estate area 24 to be electrically connected to the first buffer 12. In this regard, *Yoshitake* may include bridging traces or other mechanisms to electrically connect the input driver 11 around the real estate area 24 to the first buffer 12.

In addition, *Yoshitake* clearly does not disclose a common area comprising an alignment link for electrically connecting a first port to a second port. Instead, *Yoshitake* discloses that the first buffer 12 is disposed at a central location of chip 10. The first buffer 12 is connected to second buffers 13A, 13B, 13C and 13D by four clock wiring lines 15A, 15B, 15C and 15D, respectively, so that an output of the first buffer 12 is imported to the second buffers 13A-D over the wiring lines 15A-D, respectively. Thus, *Yoshitake* discloses the first buffer 12 being connected to second buffers 13A-D by four clock wiring lines 15A-D, and not to a second port as defined by claim 1.

Further, *Yoshitake* does not teach, disclose or suggest a second port extending directly into a common area. Instead, *Yoshitake* discloses the first buffer 12 extending over real estates 22, 24, 25, 26 and 28 to be connected to second buffers 13A-D.

Consequently, due to the failure of *Yoshitake* and Applicant Admitted Prior Art (Figs. 1 and 2) to teach, disclose or suggest all of the elements of claim 1, the combination of *Yoshitake* and Applicant Admitted Prior Art does not render claim 1 obvious. Applicants respectfully request allowance of claim 1.

Claims 2-4

Applicants respectfully submit that claims 2-4 depend from claim 1 and should be allowed as a matter of law for at least this reason. *In re Fine*, USPQ2d 1596, 1600 (Fed. Cir. 1988).

Claim 17

Claim 17 recites:

> 17. An integrated circuit comprising:
> a first port for outputting a signal;
> a second port for receiving said signal;
> ***a common area comprising an alignment means for electrically connecting said first port with said second port;***
> ***said first port extends directly into said common area from a first area; and***
> ***said second port extends directly into said common area from a second area.***

(Emphasis Added)

Applicants respectfully submit that the combination of Applicant Admitted Prior Art and *Yoshitake* fails to teach, disclose or suggest at least the above-emphasized elements. Particularly, the combination fails to teach, disclose or suggest the elements of a common area comprising an alignment link for electrically connecting a first port with a second port, the first port extending directly into the common area from a first area, and the second port extending directly into the common area from a second area.

In preliminarily rejecting claim 17, the Office Action recites:

> Regarding claims 1 and 17, Applicant Admitted Prior Art disclose an integrated circuit (Figs. 1 and 2) comprising:
> a first port 10-13 for outputting a signal;
> a second port 14, 15, 16 and 17 for receiving the signal;
> a common area 35 comprising an alignment link 30, 31, 32 and 33 for electrically connecting the first port with the second port;
> the second port extends directly into the common area from a second area;
> the alignment link comprises a signal buffer for buffering a signal traveling along the alignment link between the first port and the second port. However, Applicant Admitted Prior Art (Figs. 1 and 2) fail to disclose the first port extends directly into the common area from a first area.
> Yoshitake discloses a clock distribution circuit for a semiconductor integrated circuit comprising:
> an input driver 11 for outputting a signal; a buffer 12 for receiving an output of the driver 11 (fig. 1, column 7, lines 10-20), wherein the driver 11 extends directly from the first area into the buffer 12 to provide a clock distribution circuit and can realize reduction in skew. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Applicant Admitted Prior Art (Figs. 1 and 2) to provide the driver 11 extends directly from the first area into the buffer 12, as shown by Yoshitake to make a direct contact and avoid the links.

(Office Action, pp. 2-3)

As noted above, the Office Action admits that Applicant Admitted Prior Art (Figs. 1 and 2) fails to disclose the first port extending directly into a common area from a first area. In this regard, the Office Action refers to *Yoshitake*. However, *Yoshitake* does not teach, disclose or suggest the element of a first port extending directly into a common area. Instead, *Yoshitake* discloses a clock distribution circuit for a semiconductor integrated circuit comprising an input driver 11 for receiving a clock signal from the outside, which the input driver 11 is connected to a first buffer 12 where the connection crosses over a real estate 24. The input driver 11 is connected to the first buffer 12 by clock wiring line 19 so that an output of the input driver 11 is input into the first buffer 12 over the clock wiring line 19 (column 7, lines 22-26).

Yoshitake clearly does not teach, disclose or suggest a first port extending directly into a common area from the first area. Instead, Fig. 1 of *Yoshitake* shows a wiring diagram of a circuit and not a physical layout of the circuit. *Yoshitake* discloses an input driver 11 by clock wiring line 19 extending over a real estate area 24 to be electrically connected to the first buffer 12. In this regard, *Yoshitake* may include bridging traces or other mechanisms to electrically connect the input driver 11 around the real estate area 24 to the first buffer 12.

In addition, *Yoshitake* clearly does not disclose a common area comprising an alignment link for electrically connecting a first port to a second port. Instead, *Yoshitake* discloses that the first buffer 12 is disposed at a central location of chip 10. The first buffer 12 is connected to second buffers 13A, 13B, 13C and 13D by four clock wiring lines 15A, 15B, 15C and 15D, respectively, so that an output of the first buffer 12 is imported to the second buffers 13A-D over the wiring lines 15A-D, respectively. Thus, *Yoshitake* discloses the first buffer 12 being connected to second buffers 13A-D by four clock wiring lines 15A-D, and not to a second port as defined by claim 17.

Further, *Yoshitake* does not teach, disclose or suggest a second port extending directly into a common area. Instead, *Yoshitake* discloses the first buffer 12 extending over real estates 22, 24, 25, 26 and 28 to be connected to second buffers 13A-D.

Consequently, due to the failure of *Yoshitake* and Applicant Admitted Prior Art (Figs. 1 and 2) to teach, disclose or suggest all of the elements of claim 17, the combination of *Yoshitake* and Applicant Admitted Prior Art does not render claim 17 obvious. Applicants respectfully request allowance of claim 17.

Claims 18 and 20

Applicants respectfully submit that claims 18 and 20 depend directly from independent claim 17. Since independent claim 17 should be allowed, as argued hereinabove, pending dependent claims 18 and 20 should also be allowed as a matter of law for at least this reason. *In re Fine*, USPQ2d 1596, 1600 (Fed. Cir. 1988).

Claim 6

Claim 6 recites:

> 6. An integrated circuit comprising:
> a first port located in a first area of integrated circuit real estate, for outputting a signal;
> a second port located in a second area of integrated circuit real estate, for receiving said signal;
> ***a common area comprising an alignment link for electrically connecting said first port with said second port;***
> ***said first port extends directly into said common area from a first area;***
> ***said second port extends directly into said common area from a second area;***
> said alignment link comprises a signal buffer for buffering a signal traveling along said alignment link between said first port and said second port; and
> said integrated circuit real estate comprises multi-levels.

(Emphasis Added)

Applicants respectfully submit that the combination of Applicant Admitted Prior Art, *Yoshitake* and *Mizuno* fails to teach, disclose or suggest at least the above-emphasized elements. Particularly, the combination fails to teach, disclose or suggest the elements of a common area comprising an alignment link for electrically connecting a first port with a second port, the first port extending directly into the common area from a first area, and the second port extending directly into the common area from a second area.

In preliminarily rejecting claim 6, the Office Action recites:

> Regarding claims 6 and 7, Applicant Admitted Prior Art disclose an integrated circuit (Figs. 1 and 2) comprising:
> a first port 10-13 for outputting a signal;
> a second port 14, 15, 16 and 17 for receiving the signal;
> a common area 35 comprising an alignment link 30, 31, 32 and 33 for electrically connecting the first port with the second port;
> the second port extends directly into the common area from a second area;

the alignment link comprises a signal buffer for buffering a signal traveling along the alignment link between the first port and the second port. However, Applicant Admitted Prior Art (Figs. 1 and 2) fail to disclose the first port extends directly into the common area from a first area.

Yoshitake discloses a clock distribution circuit for a semiconductor integrated circuit comprising:

an input driver 11 located in a first area of integrated circuit real [estate], for outputting a signal; a buffer 12 (fig. 1, column 7, lines 10-20), wherein the driver 11 extends directly from the first area into the buffer 12 to provide a clock distribution circuit and can realize reduction in skew. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Applicant Admitted Prior Art (Figs. 1 and 2) to provide the driver 11 extends directly from the first area into the buffer 12, as shown by Yoshitake to make a direct contact and avoid the links.

Applicants' priort art (figs.1-2) and Yoshitake fail to disclose the integrated circuit real estate comprises multi-levels. Mizuno et al. disclose the integrated circuit (Figs 1, 21 and abstract) comprises multi-levels wherein the multi-levels comprise a semiconductor level and a wiring level, the semiconductor level forms a buffer and control circuit so that the frequency of the oscillation output corresponds to the frequency of the clock signal (abstract) and the wiring levels 110, 11, 112, 113 (column 2, lines 55-61) provide the power supply voltage to the circuit block 300 (Fig. 1). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the ICs of Applicants' prior art (figs. 1 and 2) and Yoshitake such that the integrated circuits real estate comprise multi-levels to maintain the frequency of the signal from the clock to the oscillation and provide the power supply voltage to the circuit block shown by Mizuno et al.

(Office Action, pp. 3-4)

As noted above, the Office Action admits that Applicant Admitted Prior Art (Figs. 1 and 2) fails to disclose the first port extending directly into a common area from a first area. In this regard, the Office Action refers to *Yoshitake*. However, *Yoshitake* does not teach, disclose or suggest the element of a first port extending directly into a common area. Instead, *Yoshitake* discloses a clock distribution circuit for a semiconductor integrated circuit comprising an input driver 11 for receiving a clock signal from the outside, which the input driver 11 is connected to a first buffer 12 where the connection crosses over a real estate 24. The input driver 11 is connected to the first buffer 12 by clock wiring line 19 so that an output of the input driver 11 is input into the first buffer 12 over the clock wiring line 19 (column 7, lines 22-26).

Yoshitake clearly does not teach, disclose or suggest a first port extending directly into a common area from the first area. Instead, Fig. 1 of *Yoshitake* shows a wiring diagram of a

circuit and not a physical layout of the circuit. *Yoshitake* discloses an input driver 11 by clock wiring line 19 extending over a real estate area 24 to be electrically connected to the first buffer 12. In this regard, *Yoshitake* may include bridging traces or other mechanisms to electrically connect the input driver 11 around the real estate area 24 to the first buffer 12.

In addition, *Yoshitake* clearly does not disclose a common area comprising an alignment link for electrically connecting a first port to a second port. Instead, *Yoshitake* discloses that the first buffer 12 is disposed at a central location of chip 10. The first buffer 12 is connected to second buffers 13A, 13B, 13C and 13D by four clock wiring lines 15A, 15B, 15C and 15D, respectively, so that an output of the first buffer 12 is imported to the second buffers 13A-D over the wiring lines 15A-D, respectively. Thus, *Yoshitake* discloses the first buffer 12 being connected to second buffers 13A-D by four clock wiring lines 15A-D, and not to a second port as defined by claim 6.

Further, *Yoshitake* does not teach, disclose or suggest a second port extending directly into a common area. Instead, *Yoshitake* discloses the first buffer 12 extending over real estates 22, 24, 25, 26 and 28 to be connected to second buffers 13A-D.

As noted above, the Office Action admits that Applicant Admitted Prior Art (Figs. 1 and 2) and *Yoshitake* fail to disclose the integrated circuit real estate comprises multi-levels. In this regard, while *Mizuno* may disclose multi-level integrated circuits, the combination of Applicant Admitted Prior Art (Figs. 1-2), *Yoshitake* and *Mizuno* still fails to disclose all elements of claim 6, and thus the combination does not render claim 6 obvious. Consequently, Applicants respectfully request allowance of claim 6.

Claims 7-10

Applicants respectfully submit that claims 7-10 use independent claim 6 as a base claim. Since independent claim 6 should be allowed, as argued hereinabove, pending dependent claims 7-10 should also be allowed as a matter of law for at least this reason. *In re Fine*, USPQ2d 1596, 1600 (Fed. Cir. 1988).

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicants respectfully submit that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 1-10, 17, 18 and 20 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

M. Paul Qualey
Registration No. 43,024

THOMAS, KAYDEN,
HORSTEMEYER & RISLEY, L.L.P.
Suite 1750
100 Galleria Parkway N.W.
Atlanta, Georgia 30339
(770) 933-9500

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Commissioner for Patents, Washington D.C. 20231, on

October 10, 2002.

Cory Rose

Signature -